

STEPHEN KEMPF

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Objective:

To attain a full-time position where I can apply my knowledge of computer engineering as a digital circuit design engineer.

Education:

University of Illinois at Urbana-Champaign:

B.S. in Computer Engineering - May 2005
M.S. in Computer Engineering - May 2007

August 2001 - Present

GPA: 3.97 / 4.0

GPA: 3.78 / 4.0

Work History:

Intel Corporation – Summer Intern:

Summer 2006

- Modified HDL code to enable new verification techniques. Wrote several Perl scripts to assist with code conversion. Used custom simulation tools to verify functionality of modified code.

UIUC ECE Dept. - Graduate Teaching Assistant:

Spring 2005 - Present

- Supervised & Graded two laboratory sections for Digital Systems Lab. As Head TA (Summer 2005-Present), revised, rewrote, & tested (in VHDL) portions of the course lab manual.

nVIDIA – Summer Intern:

Summer 2004

- Tested new graphics processing unit in preparation for production. Tests included verifying secondary chip functions, screening engineering sample chips, determination of maximum operating frequency under temperature stress, and verification of onboard DRAM timings.

Projects:

Design of Fault-Tolerant Digital Systems Term Project:

Spring 2006

- Designed an error detection method using two PowerPC 405 cores by comparing memory accesses. Written in VHDL targeting a Xilinx Virtex-II FPGA (not physically implemented due to lack of available hardware); experimental data gathered via simulation (ModelSim).

Microcomputer Laboratory Final Project:

Spring 2005

- Designed a video game shooter implemented on a Xilinx Virtex-II Pro FPGA. Personal responsibilities included overall planning and implementation of GIF decode algorithm.

Computer Organization and Design Final Project:

Spring 2004

- Designed a simple processor with a 5-stage pipelined datapath, an L2 split cache memory system, and 15 instructions (including conditional branch and subroutine call/return).

Selected Other Coursework:

Physical VLSI Design

Spring 2007

Digital Integrated Circuit Design

Fall 2006

Design of Fault-Tolerant Digital Systems

Spring 2006

Computer Architecture

Fall 2005

Logic Design

Spring 2005

Introduction to VLSI System Design

Fall 2004

IC Device Theory & Fabrication

Fall 2004

Activities:

AMD Jerry Sanders Design Competition:

January 2003 – Present

- Took on responsibilities of webmaster committee position fall 2003. Remodeled and maintained web site (2004-present) (<http://dc.cen.uiuc.edu/>).
- Wrote 2004 competition rules & resolved rules disputes.
- Constructed course for 2003 - 2007 competitions with other committee members & volunteers.

Computer Experience Summary:

Microsoft Windows, MS Office, Linux; VHDL, Verilog, ModelSim, Mentor Graphics, HDL Designer, Various other CAD tools; C/C++, Perl, Java, Assembly (x86, PowerPC); HTML, CSS, JavaScript